AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 7, at line 10 with the following amended paragraph:

If the control circuit determines that the calculated average power is higher than the intermediate reference value, it produces a down-shift control signal that causes the bit shifter 5 to select from an interpolated M-bit sequence an L-bit sequence {(i-j+1) through (i-j+L)} that is shifted upwards by ~~"k"~~ "j" bits with respect to the default bit positions as illustrated in Fig. 3, where the integer "j" represents the difference between the calculated average power and the intermediate reference value. Control circuit 4 proceeds to control the amplifier 7 by decrementing its gain by an integral multiple of 6 dB, i.e., 6 dB times the integer "j". Since the j-bit upward-shifted L-bit sequence is 2^j times greater then the L-bit sequence which would be selected from the default bit positions, the complementary decrement of the amplifier gain by a factor 2^j controls the CNR value of the current higher-than-reference signal at the same value which would be obtained when the average power of the input signals is equal to the reference value.